Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	142	174/255-265.ccls. and resin with (print$3 wir$3 circuit) near3 (board substrate) with (mould$3 mold$3)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2005/11/08 15:54
L2	95	174/255-265.ccls. and resin with (print$3 wir$3 circuit) near3 (board substrate) with (mould$3 mold$3) and (mount$3 attach$3) near3 (ic chip semiconductor device)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2005/11/08 15:57
L3	3	"29"/$.ccls. and (insulat$3 dielectric resin) with (print$3 wir$3 circuit) near3 (board substrate) with (mould$3 mold$3) with (pour$3 inject$3) and (mount mounting mounted attach$3) near3 (ic chip semiconductor device) and (conduct$3 metal$3) near2 (member post pin connector interconnector) with (arrang$4 place placing)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2005/11/08 16:02
L4	3	"29"/$.ccls. and (insulat$3 dielectric resin) with (print$3 wir$3 circuit) near3 (board substrate) with (mould$3 mold$3) with (fill filling filled pour$3 inject$3) and (mount mounting mounted attach$3) near3 (ic chip semiconductor device) and (conduct$3 metal$3) near2 (member post pin connector interconnector) with (arrang$4 place placing)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2005/11/08 16:03
L5	2	"264"/$.ccls. and (insulat$3 dielectric resin) with (print$3 wir$3 circuit) near3 (board substrate) with (mould$3 mold$3) with (fill filling filled pour$3 inject$3) and (mount mounting mounted attach$3) near3 (ic chip semiconductor device) and (conduct$3 metal$3) near2 (member post pin connector interconnector) with (arrang$4 place placing)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2005/11/08 16:04

L6	5	"174"/$.ccls. and (insulat$3 dielectric resin) with (print$3 wir$3 circuit) near3 (board substrate) with (mould$3 mold$3) with (fill filling filled pour$3 inject$3) and (mount mounting mounted attach$3) near3 (ic chip semiconductor device) and (conduct$3 metal$3) near2 (member post pin connector interconnector) with (arrang$4 place placing)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2005/11/08 16:05
L7	6	"361"/$.ccls. and (insulat$3 dielectric resin) with (print$3 wir$3 circuit) near3 (board substrate) with (mould$3 mold$3) with (fill filling filled pour$3 inject$3) and (mount mounting mounted attach$3) near3 (ic chip semiconductor device) and (conduct$3 metal$3) near2 (member post pin connector interconnector) with (orient$3 configur$3 arrang$4 place placing)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2005/11/08 16:06
L8	9	"439"/$.ccls. and (insulat$3 dielectric resin) with (print$3 wir$3 circuit) near3 (board substrate) with (mould$3 mold$3) and (mount mounting mounted attach$3) near3 (ic chip semiconductor device) and (conduct$3 metal$3) near2 (member post pin connector interconnector) with (orient$3 configur$3 arrang$4 place placing)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2005/11/08 16:07
L9	9	"29"/$.ccls. and (insulat$3 dielectric resin) with (print$3 wir$3 circuit) near3 (board substrate) with (mould$3 mold$3) and (mount mounting mounted attach$3) near3 (ic chip semiconductor device) and (conduct$3 metal$3) near2 (member post pin connector interconnector) same (orient$3 configur$3 arrang$4 place placing)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2005/11/08 16:08